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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/027,618	10/22/2001	Cynthia M. Merkin	M-11898 US	2972

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EXAMINER	
CHUNG, JI YONG DAVID	
ART UNIT	**PAPER NUMBER**
2143	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/027,618	MERKIN, CYNTHIA M.	
	Examiner	Art Unit	
	Ji-Yong D. Chung	2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/25/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1 and 3-17** are rejected under 35 U.S.C. 102(e) as being anticipated by Kosugi et al. (Kosugi hereinafter).

With regard to **claim 1**, Kosugi shows the method comprising:

configuring the system management controller to monitor a task of writing data to an event log, the task being executed by a Basic Input Output System (BIOS) program in response to the failure [See item 88, Fig. 2 for the system management controller. BIOS program is not explicitly spelled out. However, its existence within Kosugi can be inferred from the mention of BIOS log (see paragraph 0029), POST (see paragraph 0029), and the fact that CPU's are Intel Architecture (paragraph 0029) which use BIOS. The task of writing the log is performed by BIOS program ("BIOS log")];

monitoring the task for completion [See paragraph 0030, which indicates that the system controller is notified of errors in BOOT processing. In other words, it is monitoring BIOS sequence, which includes BIOS logging]; and

accessing the event data if the task fails to complete [See paragraph 0030. It describes system controller 88 accesing the BIOS log in non-volatile storage in the case of failure].

With regard to **claim 3**, Kogusi shows that monitoring the task comprises:

setting a configurable time of a watchdog timer, the task being configured to access the event data, and write the data to the event log in response to the event data, the task being completed within the configurable time set in the watchdog timer [See Figs. 7A and 7B and paragraph 0035 for the description of IMP board, which acts on behalf of the controller 88. The paragraphs 0035 and 0038 describe "configuring" (or setting) of the timers. The task of writing the event log has been discussed with respect to claim 1. Note that what is being written has to be "event data."];

receiving an indication from the BIOS program on completion of the task [See POST diagnosis UNIT in item 100 ("BIOS") in Fig. 3A. See Fig. 7A for problem notification process. Starting of BOOT (which is started by the BIOS) is used as notification that POST (which includes logging) has terminated].

With regard to **claim 4**, Kosugi shows *that the task fails to complete when the task fails to receive the indication from the BIOS program.* See step S4 in Fig. 7A, for when the timer expires before BOOT. See paragraph 0035 for various timer expirations descriptions.

With regard to **claim 6**, Kosugi shows that *the event data is stored in a memory of the computer system by a controller device included in the computer system.* See Fig. 2A, which

shows the nonvolatile memory 78, which is on the computer system. Paragraph 0034 indicates that the event log is stored in nonvolatile memory 78. Note that CPU, items 64-1, ("controller device") executes BIOS (and thus BIOS logging)].

Claims 7 and 8 refer to two controllers: *memory controller and I/O controller.* Kosugi meet the limitations in two ways. First, note that CPU's generally control memory and I/O. Therefore, Kosugi's CPU can be viewed as both memory controller and I/O controller. Second, hardware specific memory controllers and I/O controllers are generally inherent in most motherboards (For example, see descriptions of Intel 865D, which are involved in writing of data to memory. Baseboard in Kosugi corresponds to motherboard].

With regard to **claim 9**, Kosugi shows that *the system management controller accesses the event data over a system bus of the computer system.* See Fig. 2A and PCI bus 66 as well as well I2C bus 84-1 and 84-2.

With regard to **claim 10**, Kosugi shows an *SMBus.* I2C Bus 84-1 is the SMBus.

With regard to **claim 11**, Kosugi shows *the system management controller writing the event log in response to accessing the event data.* The BIOS log in nonvolatile memory 78 is transferred and written to nonvolatile memory 140 of the Server Management Support Board 36. See the end of paragraph 0034.

With regard to **claim 12**, Kosugi shows that *writing the event log occurs over a system bus of the computer system*. See PCI bus 66 in Fig. 6A. Server Management Board 36 is implemented as a PCI board, and therefore it uses PCI bus.

With regard to **claim 13**, its limitation has been discussed with respect to claim 10.

With regard to **claim 14**, two of its limitations have not been discussed. They are:

configuring the watchdog timer to allow the BIOS program to complete in absence of a second failure. Kosugi shows this limitation in Fig. 7A. The flow chart shows that when a particular failure occurs twice, the steps in Fig. 7A are re-traversed. Specifically, note the path through S1, S2, S3, S5, S8 and S10, and then returning to S1. On the second traversal, the timer will be restarted again at S5.

determining whether the execution of the BIOS program caused the second failure, the second failure forcing the watchdog timer to expire. The expiration in S8, Fig. 7A indicates the trouble with booting and BIOS and thus the second failure.

With regard to **claim 15**, Kosugi shows that *the second failure is substantially similar to the first failure*. In traversing Fig. 7A diagram, the second failure (which is the same as the first one) will occur again and cause the reboot.

With regard to **claim 16**, Kosugi shows that *the second failure occurs while a processor included in the computer system operates in a SMM mode*. System Management Mode occurs

during pre-boot. Fig. 7A shows that the second failure, at the second traversal of the steps in Fig. 7A, occurs prior to the start of the BOOT.

Claim 17 substantively restates the limitations of claims 1 and 3-16, but in apparatus form rather than in method form. The reasons for the rejections of claims 1 and 3-16 apply to claim 17. Therefore, claim 17 is rejected for substantially the same reasons.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 2, 18 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kosugi in view of Davis.

With respect to **claim 2**, Kosugi does not show that *the failure generates a system management interrupt and the BIOS program is triggered in response to the system management interrupt.* However, Davis shows the generation of both system interrupt and triggering of the timer interrupt in lines 12-37, column 4. Note that Kosugi shows the failure is written in BIOS log.

The motivation for using interrupts to signal failure in Kosugi is that Davis suggests the use of interrupts for error detection in pre-boot operations. See lines 12-37, column 4.

Claims 18 and 19 substantively restate the limitations of claims 1-17, but in apparatus form rather than in method form. The reasons for the rejections of claims 1-17 apply to claims 18 and 19 with respect to its constituent limitations. Note that Davis illustrates timer interrupt being set upon the first failure.

The rationale for the obviousness rejection of claim 2 holds for claims 18 and 19.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji-Yong D. Chung whose telephone number is (571) 272-7988. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Wiley can be reached on (571) 272-3923. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ji-Yong D. Chung
Patent Examiner
Art Unit: 2143

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